A LOW PHASE NOISE MMIC/HYBRID 3.0W AMPLIFIER AT X-BAND

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ABSTRACT

A power amplifier characterized by low phase modulation of the signal is important for Doppler radar systems in signal detection. Phase noise performance of -145 dBc/Hz measured at 10 kHz away from the carrier has been achieved with a MMIC/hybrid FET 3.0W X-Band amplifier. A comparison with other power amplifiers such as IMPATTs, TWTs, and magnetrons shows that the MMIC/hybrid power amplifier has a lower phase noise level. It was found experimentally that the non-linearity operation of an amplifier and the instabilities of DC regulators are the primary sources of phase noise corruption. Circuit descriptions, performances and discussion of the phase noise behavior of individual stages and of the integrated amplifier module are presented.

INTRODUCTION

High phase noise level of active and passive components such as amplifiers, oscillators, and mixers are the limiting factor of signal detection in Doppler radar systems. Phase noise can partially or completely mask the signal reflected from a moving target. Recent advances of FET and MMIC technologies have made possible the design of a compact size 3.0W, MMIC/hybrid, power amplifier at X-band that can provide a low phase noise level.

In order to enhance the sensitivity of signal detection, it is crucial that phase noise corruption is minimized. To achieve that objective, the behavior of near carrier noise of a power amplifier module must be understood; it is described in this paper.

AMPLIFIER DESIGN

Amplifier Design Concept

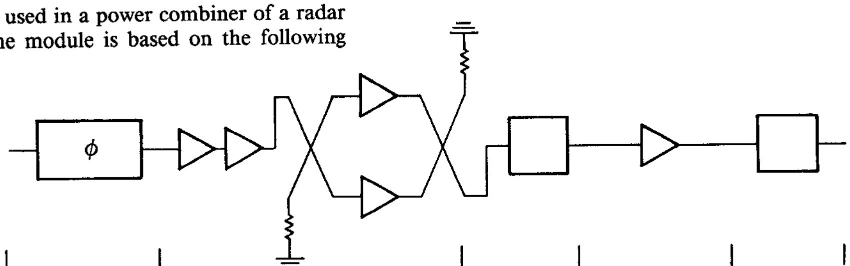
Since this amplifier is used in a power combiner of a radar transmitter, the design of the module is based on the following guidelines. First, the module is required to have a low additive phase noise level. Secondly, in the event of multiple amplifier failures in a combiner, a built-in-test circuit (BIT) is required to shut down the amplifier in question. Finally, to ensure proper signal summing, a phase adjustment capability is necessary.

A block diagram of the amplifier module with its projected gain and power budgets is shown in Figure 1. The amplifier is pictured in Figure 2. The line-up consists of a phase trimmer, a single ended two-stage MMIC driver, a balanced medium power amplifier, and a high power stage in cascade. A BIT circuit is included to monitor the output power of the integrated unit.

Circuit Design

Circuit designs and performances of individual stages of the amplifier module are highlighted below.

First, the MMIC driver stage consists of a single MMIC amplifier chip and two fifty-ohm transmission lines in alumina for input and output RF connections. The chip design is single ended and has a 600 μm FET driving a 1200 μm FET. The design bandwidth is 3 GHz to allow for frequency shifts due to process variations. The chip itself measures 74 x 104 x 4 mils. The amplifier chips are processed on three-inch-diameter GaAs wafers. An off-chip, 27,000 pF capacitor is used to ensure stability in the combined drain bias lines. The gates are biased through Ti/Pt resistors on the chip, which also act as stabilizing elements at the expense of some gain. Best data to date shows over 26 dBm of output power at 8 dB gain. A more detailed circuit description can be found in Reference [1].



	PHASE TRIMMER	MMIC DRIVER	HYBRID RPK 9030	NEG REG	HYBRID FUJITSU	BIT	
25°C							
GAIN (dB)	-0.5	9	6	-0.2	6	-0.2	20.1
PWR (dBm)	13.9	13.4	22.4	28.4	28.2	34.2 34	
85°C							
GAIN (dB)	-0.5	7.44	5.22	-0.2	5.22	-0.2	16.98
PWR (dBm)	17.02	16.52	23.96	29.18	28.98	34.2 34	
-54°C							
GAIN (dB)	-0.5	11.05	7.03	-0.2	7.03	-0.2	24.21
PWR (dBm)	9.79	9.29	20.34	27.37	27.17	34.2 34	

Figure 1. Block Diagram of MMIC/Hybrid Power Amplifier

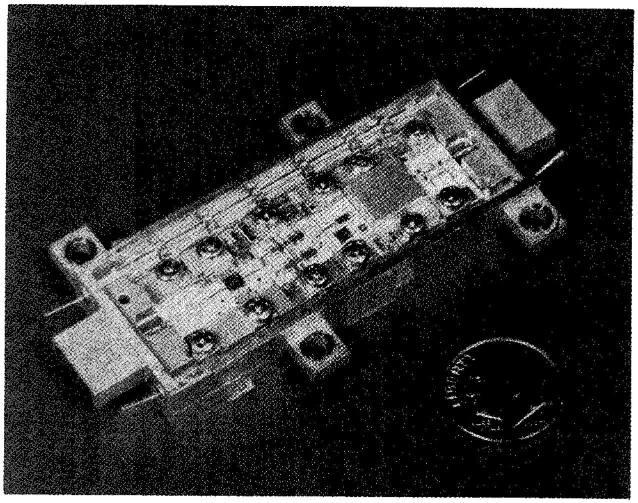


Figure 2. Integrated Amplifier Module

The next stage is a balanced medium power stage using Raytheon RPK 9030 discrete FETs. Each chip has a gate periphery of 1600 μm and an output power of 30 dBm with an associated gain of 8 dB at X-band. A balanced approach is used for this stage to minimize VSWR interactions between the MMIC driver and the output stage, which are both in a single ended configuration. The gate matching network was designed based on measured S-parameters of the RPK 9030 device; it has a band pass structure which consists of one shunt resonator realized by a shunt open stub and a quarter wave transformer. The drain circuit design was based on large signal characteristics of the device. This medium power stage yielded a power of 30 to 31 dBm at the 1 dB point and a small signal gain of 7 ± 0.5 dB.

The final stage is a high power internally matched FET manufactured by Fujitsu. Measured data of this stage showed a small signal gain of 6.5 ± 0.5 dB and a power of 35 dBm at the 1 dB point. Gain and power responses of these three stages can be found in Figures 3, 4 and 5.

The design of the integrated amplifier is modular. Each amplifier stage was tested before assembly in the final amplifier housing. A lap-joint technique was utilized for making external RF connections from the housing to the combiner/divider assemblies in the transmitter. Thus defective amplifier modules could be replaced without needing to make and break solder connections between each module and the stripline RF power divider/combiner. The gain and output response of the integrated amplifier is shown in Figure 6. A small signal gain of 23 ± 0.5 dB and a saturated output power of 35 ± 0.5 dBm at 2-3 dB compression were measured over 15 percent bandwidth at X-band.

AMPLIFIER PHASE NOISE

Noise Measurement

The quadrature phase detection technique reported in References [2] and [3] was used for measuring phase noise. The near carrier noise of the amplifier under test is converted to baseband noise by mixing the carrier with a reference signal of the same frequency in a double balanced mixer. When these two signals are 90 degrees out of phase, the voltage at the IF port represents the phase noise corruption of the noise system by an amplifier under test.

Figure 7 shows the noise test set-up. In the reference arm, a phase shifter is used to set the quadrature condition. The function of the air line stretcher is to ensure that both arms of the phase bridge are balanced. The adjustment of the variable at-

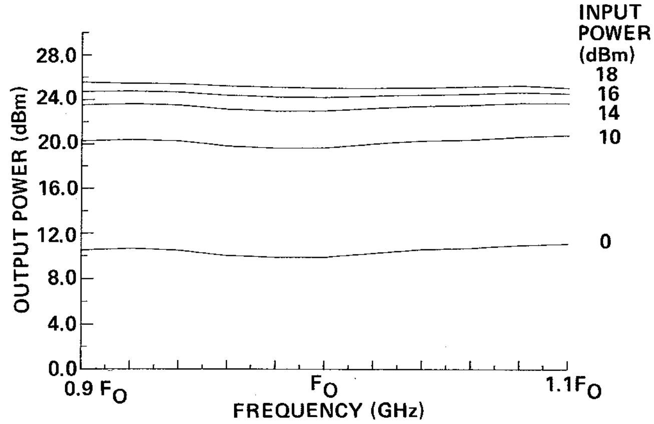


Figure 3. Small Signal Gain and Output Power of the MMIC Stage

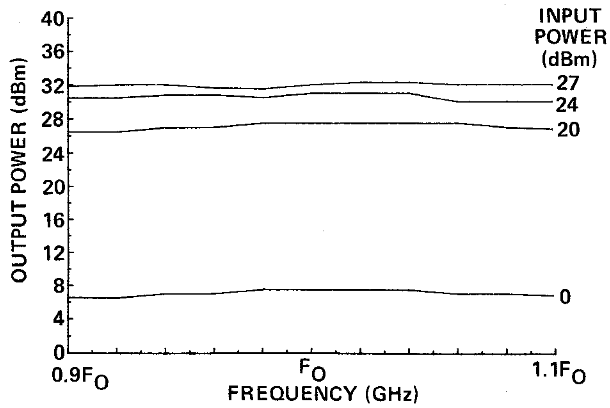


Figure 4. Small Signal Gain and Output Power of the RPK 9030 Stage

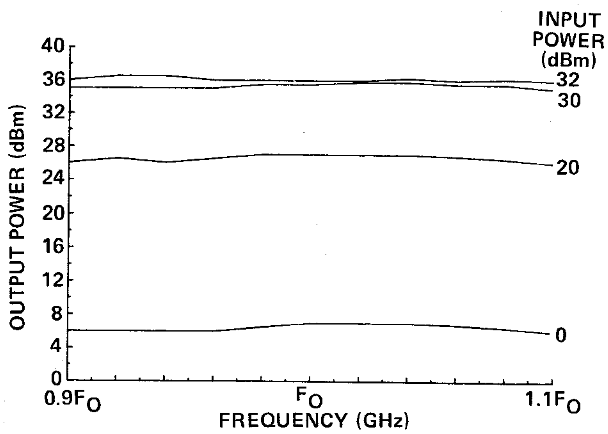


Figure 5. Small Signal Gain and Output Power of the Fujitsu Stage

tenuator VA1 enables phase noise to be characterized at various output powers of the amplifier under test. Variable attenuators VA2 and VA3 are used to maintain the same operation of the double balanced mixer throughout the noise measurement. In the quadrature condition, the RMS voltage, shown in Equation 1, at the IF port is proportional to the fluctuating phase difference $\Delta\phi_{RMS}$ between the RF and LO signals.

$$\Delta V_{RMS} = K_\phi \Delta\phi_{RMS} \quad (1)$$

K_ϕ is the phase slope of the mixer (volt/radian).

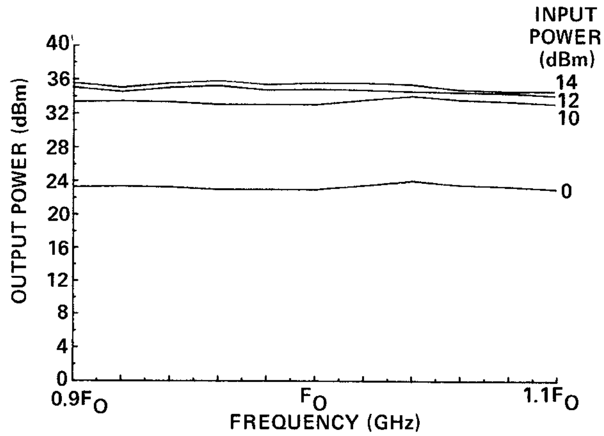


Figure 6. Small Signal Gain and Output Power of the Integrated Amplifier

The ratio of single-sideband power of phase noise in a 1 Hz bandwidth at f_m Hz away from the carrier to the total signal power is given by Reference [4]:

$$L(f_m) = \frac{1}{2} \frac{(\Delta V_{RMS})^2 \ (1Hz)}{K_\phi^2} \qquad (2)$$

The term $L(f_m)$ is dependent on two parameters $K\phi$ and ΔV_{RMS}. By maintaining a constant phase slope K_ϕ of the double balanced mixer throughout the noise measurement, the phase noise corruption $L(f_m)$ is due solely to the phase fluctuations of the amplifier under test.

Amplifier Phase Noise Behavior

The behavior of phase noise of each amplifier stage and of the integrated module is outlined below.

Phase Noise Level versus Stage Linearity. The degree of phase noise corruption by an amplifier depends on the mode of operation of that amplifier. The phase noise level of a stage can be degraded by 5 to 8 dB when that stage is driven from the linear to the saturated region. To illustrate this point, a comparison of phase noise degradation of individual stages and of the cascaded amplifier in the linear and saturated regions can be found in Table 1 and in Figures 8 and 9.

Phase Noise Level in a Cascaded Line-up. In the linear and saturated regions, the level of phase noise in a cascaded line-up is dictated by the stage having the poorest noise performance. As shown in Figures 8 and 9, the phase noise level of the cascaded amplifier module is that of the MMIC driver, since the RPK 9030 and Fujitsu stages have a lower phase noise corruption.

Phase Noise Corruption by Voltage Regulators. In Figures 8 and 9, it can be observed that two instabilities due to low frequency oscillations of the negative regulator have raised the phase noise level of the integrated amplifier in the regions of 780 kHz and 2.4 MHz away from the carrier. Elimination of these oscillations by additional filtering of the negative supply is necessary to minimize the phase noise corruption of the cascaded amplifier.

Phase Noise Comparison of Other Devices. Other possible candidates for a power amplifier at X-band include IMPATT diodes, traveling wave tubes, and magnetrons. Table 2 lists the expected phase noise performance of these devices if they were used in a similar X-band amplifier design. Phase noise performance of magnetrons and IMPATTS can be found in References [5] and [6]. As shown in Table 2, the MMIC/hybrid amplifier is at least 10 dB better in phase noise than other available devices.

DISCUSSION AND CONCLUSION

In comparison with other devices such as IMPATTs, magnetrons and TWT amplifiers, FET power amplifiers have lower phase noise level. In that respect, MMIC/hybrid power amplifiers proved to be viable for solid state transmitters used in ground radars required to operate over a wide bandwidth and having a low additive phase noise. In this paper, we have demonstrated the capability of a MMIC/hybrid amplifier that can fulfill the above requirements. A gain of 23 dB and 3.0W of output power have been obtained over a 15 percent bandwidth at X-band. At 2 to 3 dB compression, a phase noise of -145 dBc/Hz was measured at 10 kHz away from the carrier for the integrated amplifier module.

Due to the importance of near-carrier noise to radar systems, the phase noise corruption by a power amplifier should be minimized. It has been observed that the phase noise behavior of an amplifier stage is dependent on the mode of operation of that stage. With the amplifier stage operated linearly, the phase noise level remains constant. As the output power of that stage approaches the 1 dB compression point, the phase noise degradation becomes pronounced. This is due to the AM to PM conversion that becomes an important factor of the phase noise corruption. Having that in mind, the following design considerations are suggested for low phase noise of a power amplifier. First, amplifier stages should be designed so that the power at the 1 dB point is as high as possible. This would result in a minimum phase noise corruption when these stages are cascaded. Second, special attention must be given to gate and drain regulators in addition to the design of the RF stages. Any instabilities of these voltage regulators will corrupt the near carrier noise of these stages. Consequently, selection of voltage regulators that have low noise characteristics is an important step in minimizing the amplifier phase noise corruption.

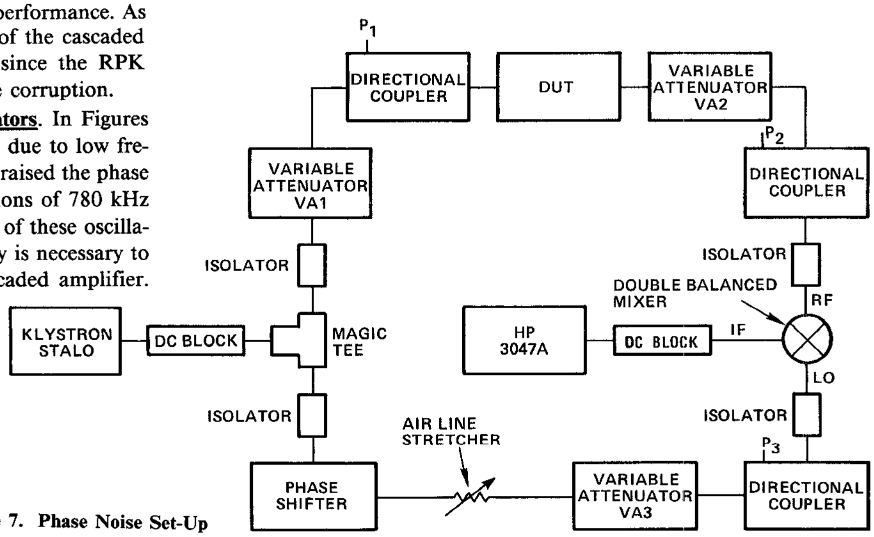


Figure 7. Phase Noise Set-Up

TABLE 1 - AMPLIFIER PHASE NOISE FOR THE LINEAR AND SATURATED REGIONS

Stage	Phase Noise Level (dBc/Hz) Measured at 10 kHz from carrier	
	Linear Region	Saturated Region
MMIC driver	-150	-145
RPK 9030 stage	-160	-152
Fujitsu Stage	-155	-150
Cascaded amplifier	-150	-145

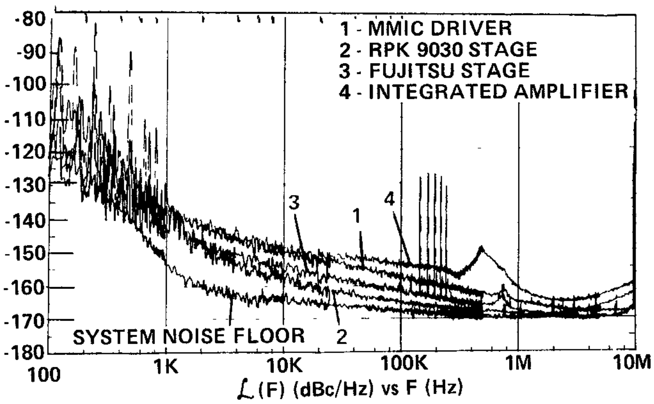


Figure 8. Phase Noise of Individual Stages and of the Integrated Amplifier Module in the Linear Region. Carrier Frequency F_o.

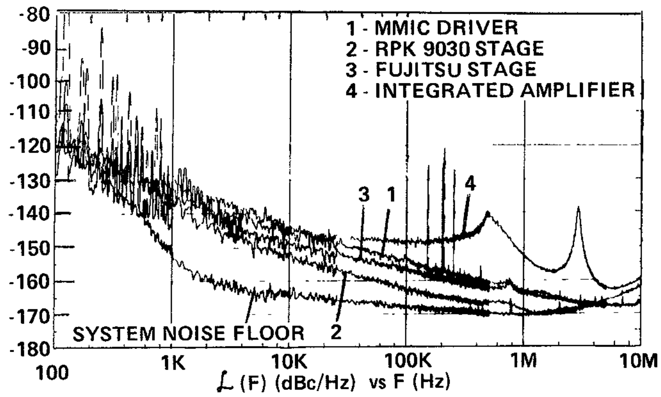


Figure 9. Phase Noise of Individual Stages and of the Integrated Amplifier Module at 2-3 dB Compression. Carrier Frequency F_o.

TABLE 2 - EXPECTED PHASE NOISE LEVELS FOR OTHER X-BAND HIGH POWER AMPLIFIERS

Phase Noise Level (dBc/Hz) Measured at 10 kHz from carrier (data for saturated output power)	
Device Type	Phase Noise
Magnetron	-80
IMPATT (pulsed)	-110 (a level of -135 dbc was obtained when the IMPATT diode was tuned at a single frequency for noise)
TWT	-110
MMIC/Hybrid Amplifier	-145

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